



# 128Kx32 CMOS High Speed Static RAM

## FEATURES

- 128Kx32 bit CMOS Static
- Random Access Memory Array
  - Fast Access Times: 12, 15, 17, 20, and 25ns
  - Individual Byte Enables
  - User Configurable Organization with Minimal Additional Logic
  - Master Output Enable and Write Control
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- Surface Mount Package
  - 68 Lead PLCC, No. 99 (JEDEC MO-47AE)
  - Small Footprint, 0.990 Sq. In.
  - Multiple Ground Pins for Maximum Noise Immunity
- Single +5V (±5%) Supply Operation

## DESCRIPTION

The EDI8L32128C is a high speed, high performance, four megabit density Static RAM organized as a 128Kx32 bit array.

Four Chip Enables, Write Control, and Output Enable provide the user with a flexible memory solution. The user may independently enable each of the four bytes, and, with minimal additional peripheral logic, the unit may be configured as a 256Kx16 or 512Kx8 array.

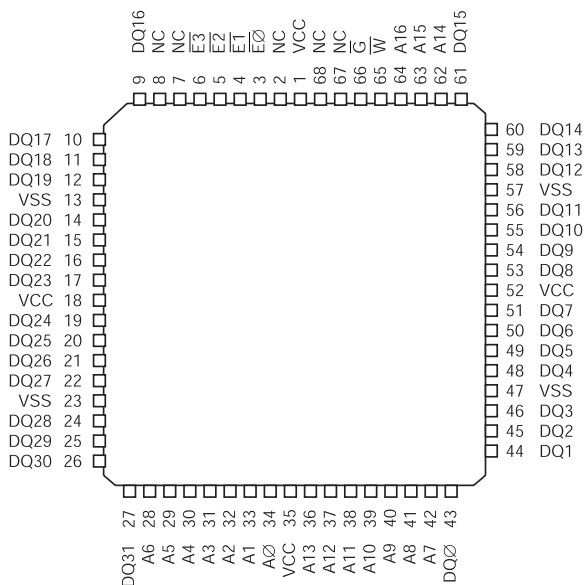
Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

The EDI8L32128C, allows 4 megabits of memory to be placed in less than 0.990 square inches of board space; a savings of 0.885 square inches over four standard 128Kx8 components.

*NOTE: Solder Reflow temperature should not exceed 230°C*

FIG. 1 PIN CONFIGURATION

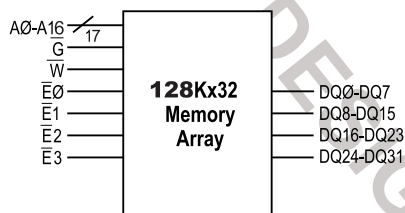
### TOP VIEW



### PIN DESCRIPTION

A0-A16	Address Inputs
$\bar{E}0-3$	Chip Enables (One per Byte)
$\bar{W}$	Master Write Enable
$\bar{G}$	Master Output Enable
DQ0-31	Common Data Input/Output
Vcc	Power (+5V±5%)
Vss	Ground
NC	No Connection

### BLOCK DIAGRAM



*NOTE: Pin 2 & 67 on the 64Kx32 (EDI8L3265C) and the 256Kx32 (EDI8L32256C) are word select pins.*



**ABSOLUTE MAXIMUM RATINGS\***

Voltage on any pin relative to Vss	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Power Dissipation	4 Watts
Output Current	20 mA
Junction Temperature, TJ	175°C

\*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**TRUTH TABLE**

$\bar{E}$	$\bar{W}$	$\bar{G}$	Mode	Output	Power
H	X	X	Standby	High Z	Icc2,Icc3,
L	H	H	Output Disable	High Z	Icc1
L	X	X	Output Disable	High Z	Icc1
L	H	L	Read	DOUT	Icc1
L	L	X	Write	DIN	Icc1

**RECOMMENDED DC OPERATING CONDITIONS**

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	Vcc	4.75	5.0	5.25	V
Supply Voltage	Vss	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.2	--	V <sub>cc</sub> +0.5	V
Input Low Voltage	V <sub>IL</sub>	-0.3	--	0.8	V

**CAPACITANCE**

(f = 1.0MHz, V<sub>IN</sub> = V<sub>CC</sub> or V<sub>SS</sub>)

Parameter	Sym	Max	Unit
Address Lines	CA	40	pF
Data Lines	CD/Q	10	pF
Write & Output Enable Lines	W, G	40	pF
Chip Enable Lines/Byte Select	E0-3	8	pF

**DC ELECTRICAL CHARACTERISTICS**

Parameter	Sym	Conditions	Typ	Max				Units
				12*	15	17	20/25	
Operating Power Supply Current	Icc1	$\bar{W} = V_{IL}, I_{IO} = 0mA,$ Min Cycle	620	720	680	640	600	mA
Standby (TTL) Supply Current	Icc2	$\bar{E} \bar{z} V_{IH}, V_{IN} - V_{IL}$ or $V_{IN} \bar{z} V_{IH}, f = 0MHz$	160	160	160	160	160	mA
Full Standby CMOS Supply Current	Icc3	$\bar{E} \bar{z} V_{CC} - 0.2V$ $V_{IN} \bar{z} V_{CC} - 0.2V$ or $V_{IN} - 0.2V$	20	20	20	20	20	mA
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = 0V to V <sub>CC</sub>				±10		µA
Output Leakage Current	I <sub>LO</sub>	V <sub>IO</sub> = 0V to V <sub>CC</sub>				±10		µA
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA	2.4					V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0mA				0.4		V

Typical: TA = 25°C, VCC = 5.0V

**AC TEST CONDITIONS**

Figure 2

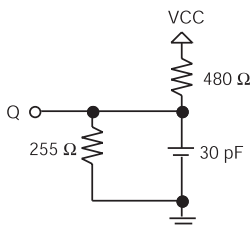
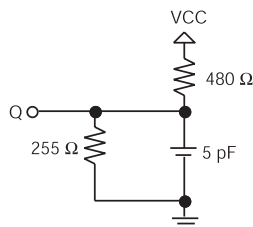


Figure 3



Input Pulse Levels	Vss to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 2

**NOTE:** For tEHQZ, tGHQZ and tWLQZ, CL = 5pF Figure 3)



AC CHARACTERISTICS - READ CYCLE

Parameter	Symbol		12ns		15ns		17ns		20ns		25n		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tAVAV	tRC	12		15		17		20		25		ns
Address Access Time	tAVQV	tAA		12		15		17		20		25	ns
Chip Enable Access Time	tELQV	tACS		12		15		17		20		25	ns
Chip Enable to Output in Low Z (1)	tELQX	tCLZ	2		3		3		3		3		ns
Chip Disable to Output in High Z (1)	tEHQZ	tCHZ		7		8		8		10		10	ns
Output Hold from Address Change	tAVQX	tOH	3		3		3		3		3		ns
Output Enable to Output Valid	tGLQV	tOE		5		6		8		8		10	ns
Output Enable to Output in Low Z (1)	tGLQX	tOLZ	2		2		2		2		0		ns
Output Disable to Output in High Z(1)	tGHQZ	tOHZ		4		5		6		8		10	ns

NOTE 1: Parameter guaranteed, but not tested.

FIG. 4 READ CYCLE 1 -  $\overline{W}$  HIGH,  $\overline{G}$ ,  $\overline{E}$  LOW

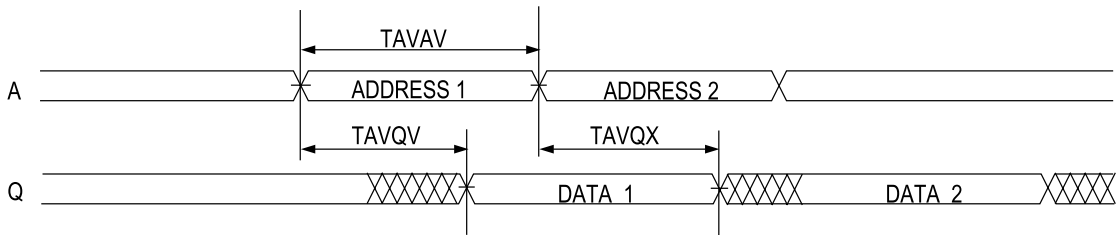
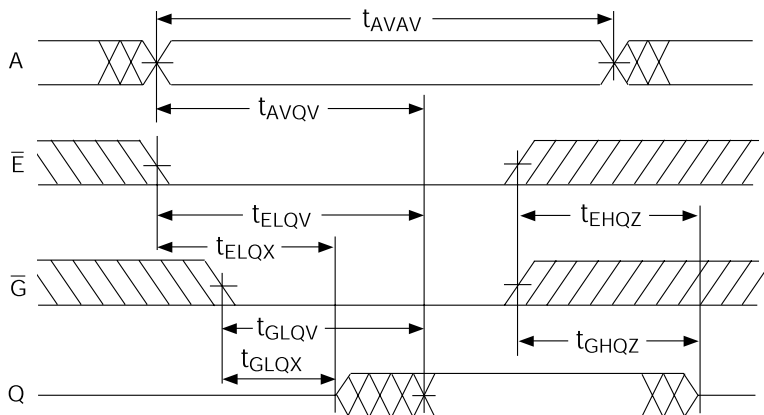


FIG. 5 READ CYCLE 2 -  $\overline{W}$  HIGH





AC CHARACTERISTICS - WRITE CYCLE

Parameter	Symbol		12ns		15ns		17ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	12		15		17		20		25		ns
Chip Enable to End of Write	tELWH	tCW	8		9		10		15		20		ns
	tELEH	tCW	8		9		10		15		20		ns
Address Setup Time	tAVWL	tAS	0		0		0		0		0		ns
	tAVEL	tAS	0		0		0		0		0		ns
Address Valid to End of Write	tAVWH	tAW	9		10		12		15		15		ns
	tAVEH	tAW	9		10		12		15		15		ns
Write Pulse Width	tWLWH	tWP	9		10		12		15		15		ns
	tWLEH	tWP	9		10		12		15		15		ns
Write Recovery Time	tWHAX	tWR	0		0		0		0		0		ns
	tEHAX	tWR	0		0		0		0		0		ns
Data Hold Time	tWHDX	tDH	0		0		0		0		0		ns
	tEHDX	tDH	0		0		0		0		0		ns
Write to Output in High Z (1)	tWLQZ	tWHZ	0	5	0	6	0	7	0	7	0	10	ns
Data to Write Time	tDVWH	tDW	5		6		8		8		12		ns
	tDVEH	tDW	5		6		8		8		12		ns
Output Active from End of Write (1)	tWHQX	tWLZ	2		2		2		2		2		ns

NOTE: Parameter guaranteed, but not tested.

FIG. 6 WRITE CYCLE 1 -  $\bar{W}$  CONTROLLED

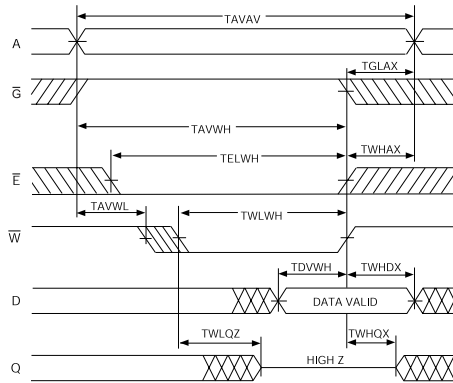
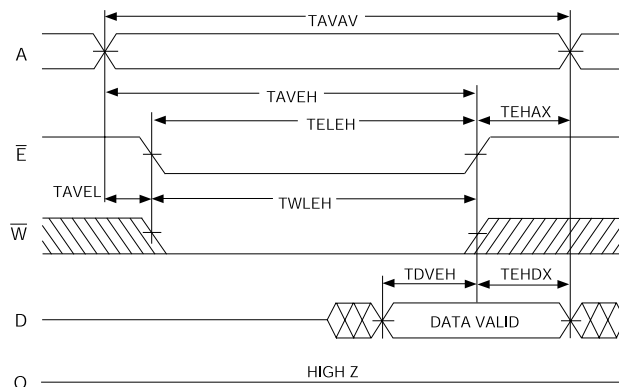


FIG. 7 WRITE CYCLE 2 -  $\bar{E}$  CONTROLLED

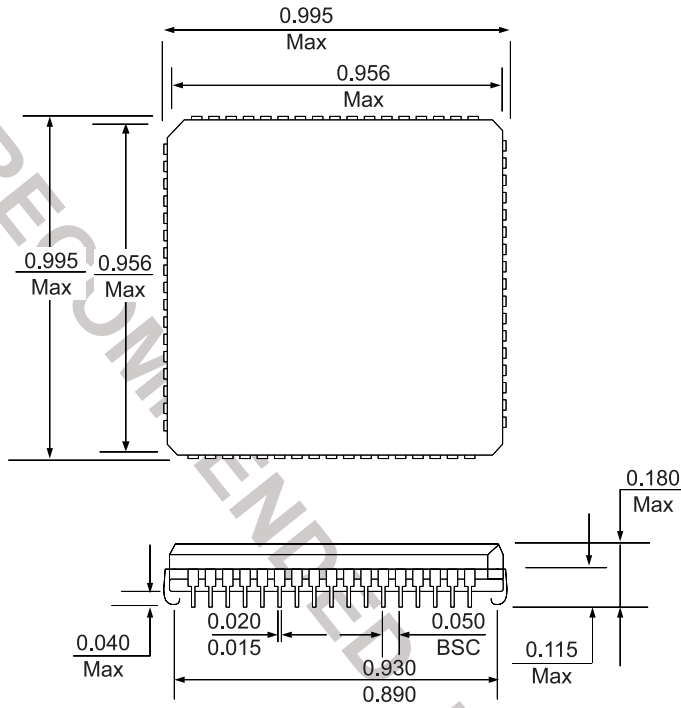




PACKAGE DESCRIPTION

PACKAGE No. 99: 68 LEAD PLCC

JEDEC MO-47AE



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

Commercial (0°C to +70°C)		
Part Number	Speed (ns)	Package No.
EDI8L32128C12AC	12	99
EDI8L32128C15AC	15	99
EDI8L32128C17AC	17	99
EDI8L32128C20AC	20	99
EDI8L32128C25AC	25	99

Industrial (-40°C to +85°C)		
Part Number	Speed (ns)	Package No.
EDI8L32128C15AI	15	99
EDI8L32128C17AI	17	99
EDI8L32128C20AI	20	99